UČNI NAČRT PREDMETA / COURSE SYLLABUS	
Predmet:	Snovanje računalniških sistemov
Course title:	Computer Systems Design

Študijski program in stopnja Study programme and level	Modul Module	Letnik Academic year	Semester Semester
Informacijske in komunikacijske tehnologije, 2. stopnja	Računalniške strukture in sistemi	1	2
Information and Communication Technologies, 2nd cycle	Computer Structures and Systems	1	2

Vrsta predmeta / Course type	Izbirni / Elective
Univerzitetna koda predmeta / University course code:	IKT2-692

Predavanja Lectures	Seminar Seminar	Sem. vaje Tutorial	Lab. vaje Laboratory work	Druge oblike	Samost. delo Individ. work	ECTS
15	**15**			**15**	**105**	**5**

**Navedena porazdelitev ur velja, če je vpisanih vsaj 15 študentov. Drugače se obseg izvedbe kontaktnih ur sorazmerno zmanjša in prenese v samostojno delo. / This distribution of hours is valid if at least 15 students are enrolled. Otherwise the contact hours are linearly reduced and transfered to individual work.*

Nosilec predmeta / Lecturer:	Doc. dr. Anton Biasizzo

Jeziki / Languages:	**Predavanja / Lectures:**	slovenščina, angleščina / Slovenian, English
	Vaje / Tutorial:	

Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:	**Prerequisites:**
Zaključen študijski program prve stopnje s področja naravoslovja, tehnike ali računalništva.	Student must complete first-cycle study programmes in natural sciences, technical disciplines or computer science.

Vsebina:	**Content (Syllabus outline):**
Snovanje digitalnih sistemov: uvod, zgodovinski razvoj področja, računalniško podprto načrtovanje, nivoji abstrakcije sistema, npr. opis na tranzistorskem nivoju, nivo logičnih vrat, nivo registrov, algoritmični model Jeziki za opis strojne opreme: uvod v jezik VHDL, hierarhično modeliranje sistema v jeziku VHDL, simulacija VHDL modela, postopek snovanja v jeziku VHDL Programirljiva logična vezja: vrste programirljivih logičnih vezij PLD, programiranje vezij PLD, kompleksna programirljiva logična vezja CPLD, programirljiva polja logična vezja FPGA	Digital system design: introduction, history of development of the area, computer aided design, system abstraction, e.g., transistor level, gate level, register-transfer level, algorithmic model Hardware description languages: introduction to VHDL, hierarchical design in VHDL, VHDL simulation, VHDL design cycle Programmable logic devices: Programmable Logic Device types, PLD programming, Complex Programmable Logic Devices CPLD, Field Programmable Gate Array FPGA Hardware design:

Snovanje strojne opreme:
snovanje strojnih jeder, ponovna uporaba strojnih jeder, snovanje večprocesorskih sistemov, strojni pospeševalniki, sistemi v čipu, omrežja na čipu
Preizkušanje digitalnih sistemov:
vloga preizkušanja, modeliranje in simulacija napak, zasnova za preizkus, vgrajeni samotest, sistemi, odporni proti napakam
Rekonfigurabilni sistemi:
sprotna delna rekonfiguracija vezij FPGA, sprotno odpravljanje okvar, snovanje zelo zanesljivih sistemov

hardware core design, hardware core reuse, multiprocessor system design, hardware accelerator design, system-on-chip, network-on-chip
Testing of digital systems: the role of testing, fault modelling, fault simulation, design for test, build in self-test, fault tolerant systems
Reconfigurable systems: dynamic partial reconfiguration of FPGA devices, on-line error recovery system, dependable system design

Temeljna literatura in viri / Readings:

Izbrana poglavja iz naslednjih knjig: / Selected chapters from the following books:

- D. Jansen, et al., *The Electronic Design Automation Handbook*. Kluwer Academic Publishers, 2003. ISBN 1-4020-7502-2
- V.A. Pedroni, *Circuit design with VHDL*. MIT Press, 2004. ISBN 0-262-16224-5
- R. Reis, M. Lubaszewski, and J.A.G. Jess, *Design of Systems on a Chip: Design and Test*. Springer, 2007. ISBN 978-0-387-32499-9
- S. Hauck, and A. DeHon, *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing*. Morgan Kaufmann, 2008. ISBN 978-0-123-70522-8
- G. De Micheli, and L. Benini, *Networks on chips*. Morgan Kaufmann, 2006. ISBN 978-0-123-70521-1

Cilji in kompetence:

Cilj predmeta je seznaniti študenta z metodami snovanja digitalnih sistemov in s snovanjem računalniških sistemov, vključno s sistemi v čipu, omrežji v čipu in rekonfigurabilnimi sistemi.

Kompetence študenta z uspešno zaključenim predmetom bodo vključevale osnovno poznavanje metod snovanja računalniških sistemov, poznavanje sodobnih računalniških struktur (sistem v čipu, omrežja v čipu, rekonfigurabilni sistemi) in znanje o snovanju le-teh.

Objectives and competences:

The goal of the course is to familiarize the student with the digital system design methods and computer system design, including system-on-chip, networks-on-chip, and reconfigurable systems.

The competencies of the students completing this course successfully would include the basic knowledge of computer system design methods, familiarity with state-of-the art computer structures (system-on-chip, networks-on-chip, reconfigurable systems), and knowledge of their design principles.

Predvideni študijski rezultati:

Študenti bodo z uspešno opravljenimi obveznostmi tega predmeta pridobili:

- pregled področja snovanja digitalnih sistemov ter naprednih računalniških struktur
- poznavanje jezika VHDL za opis digitalnih sistemov in njegovo uporabo za simulacijo ter snovanje računalniških sistemov
- sposobnost snovanja računalniških sistemov za specifične probleme
- poznavanje sistemov-v-čipu in omrežij-v-čipu

Intended learning outcomes:

Students successfully completing this course will acquire:

- Overview of the field of the digital system design and the state-of-the art computer structures
- Knowledge of the VHDL hardware description language and its use for the simulation and design of the computer system
- Ability to design application specific computer system

• poznavanje programirljivih vezij FPGA in njihovo uporabo v računalniških sistemih • poznavanje rekonfigurabilnih sistemov in sposobnost zasnove le-teh z vezji FPGA	• Knowledge of system-on-chip and networks on chip architectures • Knowledge of the programmable FPGA devices and their application on computer systems • Knowledge of the reconfigurable systems and ability to design them on FPGA devices.

Metode poučevanja in učenja:	**Learning and teaching methods:**
Predavanja, seminar, konzultacije, individualno delo	Lectures, seminar, consultancy, individual work

Načini ocenjevanja:	Delež (v %) / Weight (in %)	**Assessment:**
Seminarska naloga	50 %	Seminar work
Ustni zagovor seminarske naloge	50 %	Oral defense of seminar work

Reference nosilca / Lecturer's references:

- U. Legat, **A. Biasizzo**, and F. Novak, "SEU recovery mechanism for SRAM-based FPGAs",*IEEE trans. on nuclear science*, vol. 59, no 5, pp. 2562-2571, 2012.
- **A. Biasizzo** and F. Novak, "Hardware accelerated compression of LIDAR data using FPGA devices", *Sensors*, vol. 13, no. 5, pp. 6405-6422, 2013.
- **A. Biasizzo**, " On-line testing and recovery of systems with dynamic partial reconfiguration = Sprotno preiskušanje in popravljanje sistemov z dinamično delno rekonfiguracijo", *Informacije MIDEM*, vol. 43, no. 4, pp. 259-266, 2013
- **A. Biasizzo**, F. Novak, and P. Korošec, "A multi-alphabet arithmetic coding hardware implementation for small FPGA devices", *Journal of electrical engineering*, vol. 64, no. 1, pp 44-49, 2013
- **A. Biasizzo** and F. Novak, "Security problems of scan design and accompanying measures", *Journal of electrical engineering*, vol. 67, no. 3, pp 192-198, 2016